HSLink

Application Note | Case Study | **Technology Primer** | White Paper

Introduction

The HSLink interface is a new machine vision connectivity interface pioneered by DALSA. DALSA is working with the Camera Link 2 subcommittee to bring reference designs and a more complete specification to the table for industry use as the next generation Machine Vision interface. Contact names are provided in the appendix should you want to help develop the capability of this interface.

HSLink is designed specifically to meet the needs of all machine vision applications and therefore carries image data, configuration data and low jitter real time triggering signals over a simple network topology supporting cameras, intermediate devices and frame grabbers. The interface has taken the key strengths of Camera Link™, and added new features and functions to meet the customer demands of today and tomorrow. HSLink is designed from a system point of view, ensuring the ability to create low cost cameras and frame grabbers, while meeting the ease of use, flexibility and data reliability demanded by end customers.

Features and Benefits of HSLink

- Globally available, off-the-shelf components are used. No license or royalty fees. No chip supply issues.
- Scaleable bandwidths in 300MB/s steps from 300 to 6000 Mbytes/s, 1x to 20x configurations, while maintaining a common and consistent control interface and ease of implementation.
- Camera size is minimized.
  - Interface technology can be integrated into FPGAs rather than requiring a separate IC chip.
  - Power over HSLink is possible.
  - Protocol handles real-time triggering. No need for a separate trigger cable.
- Real-time triggering - low jitter of 3.2ns makes HSLink viable for linescan applications.
- Maintains the features of Camera Link, an industry specific connectivity solution, while using broadly-used, off-the-shelf components with development road maps for increased performance. This protocol will have a long service life.
- Lower cost data transmission across all bandwidths.
- Reliable data transmission achieved through redundant trigger codes, hardware resend capabilty, and proven technology. Hardware resend enables minimal buffer sizes suitable for inclusion in FPGAs, ie no external memory required.
- Plug and Play - Cameras are GenICam™
- General Purpose I/O are optional and supported on the camera
- Power optimized as the number of lanes needed for data transmission scales as necessary. Friendly to the environment.
- Data Forwarding - Low cost distributed image processing.
- Open development with feedback solicited and incorporated into improving the interface.
- Reference designs available to reduce implementation times.
- Designed to ensure longevity in the marketplace. Expected lifecycle is 10-20 years.

Functional Block Diagrams

To gain a better understanding of HSLink, Figure 1 provides an overview of HSLink topology from a camera perspective, and Figure 2 provides an overview of HSLink from a framegrabber perspective. Most of the discussion in this primer focuses on the camera perspective because the framegrabber perspective is very similar and uses the same technology but in reverse order.

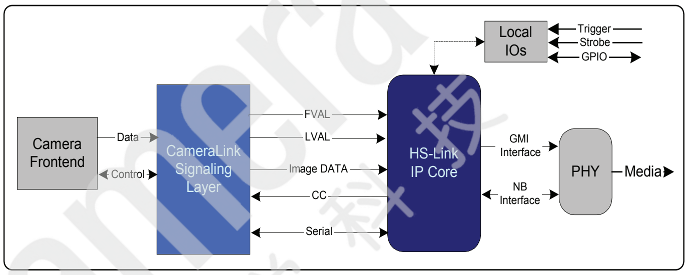


Figure 1 – Topology of HSLink from a Camera Perspective

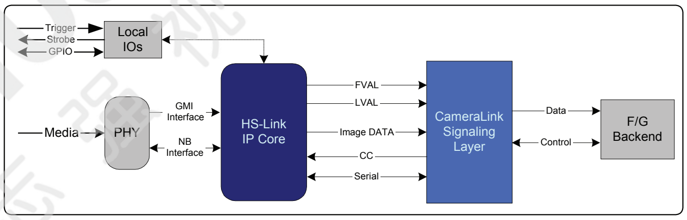


Figure 2 – Topology of HSLink from a Framegrabber perspective

As seen in both diagrams the HSLink IP Core takes in input signals that the machine vision industry understands from the CameraLink standard. On the camera side, the HSLink IP Core takes these inputs and sends them via GMII (Gigabit Media Independent Interface) and/or NBI (Nine Bit Interface), and ensures guaranteed data delivery. The PHY (SERDES chip) takes the information it receives, serializes it, and transmits it to the framegrabber via cabling. Depending upon the camera bandwidth the PHY sends the information in three potential formats that we have named NBILink, GMIILink and MixedLink. Each format has its own associated cabling and protocol.

NBILink, GMIILink and MixedLink – Cabling

Cabling is an expensive portion of a machine vision system and HSLink offers scalable bandwidths to keep the cabling costs and size appropriate to the needs of the camera, whether the camera is of high bandwidth or low bandwidth.

Three formats exist in HSLink: NBILink, GMIILink and MixedLink. Each format contains a Control Channel, and one to seven video lane channels. Figure 3, shows the diagram for the Control Channel. The control channel is comprised of one downlink communication channel (Camera to Framegrabber) and one uplink communication channel (Framegrabber to Camera), each of which are capable of carrying 300MB/s of information. The Control Channel is reserved to carry information regarding Trigger, GPIO, Ack/Nack, Command and Idle messages.

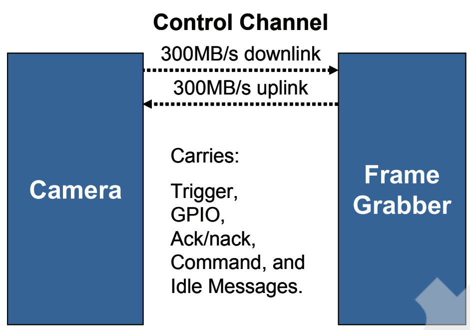


Figure 3 – Control Channel Configuration

Each video lane has a bandwidth of 300MB/s for carrying image data. As the number of video lanes increases the bandwidth increases proportionally in 300MB/s steps. For simplicity, we'll refer to these steps as x1 (300MB/s – one video lane) to x7 (2100MB/s – seven video lanes). Solutions beyond x7 are currently open for discussion and are not considered part of this primer. To minimize cabling hardware, where appropriate the downlink communication channel of the Control Channel includes video along with Trigger, GPIO, Ack/Nack, Command and Idle Messages. To better understand the differences between NBILink, GMIILink and MixedLink, we'll start with the GMIILink.

GMIILink uses off-the-shelf, multi-sourced, CX4 cable which provides eight differential pairs for use. Two of these differential pairs are used for the Control Channel. A minimum of three differential pairs have been defined as video lanes. This number can increase to six by using up all eight differential pairs in the CX4 cable. Thus, the GMIILink covers bandwidths from 3x to 6x. Figure 4, shows the GMIILink configuration.

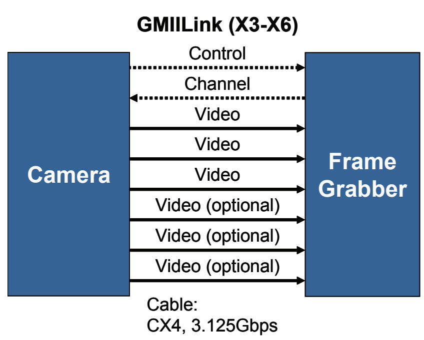


Figure 4 – GMIILink Configuration

The NBILink represents the lowest bandwidth options of x1 and x2, and thus requires the lowest cost cabling. To minimize cable needs, the NBILink combines video with the downlink Control Channel. Thus, only two physical connections are required in the cable hardware. At time of print, the connector/media for NBILink is under review, but for the x1 version both coax (RG59 x2) and Infiniband (IBx1) cables are options. In either case, these cables can carry power thereby enabling a single compact cable solution for ever-shrinking cameras and micro-camera heads. For the x2 version two Infiniband cables are proposed or three coax. Figure 5, shows diagrams of NBILink x1 and NBILink x2.

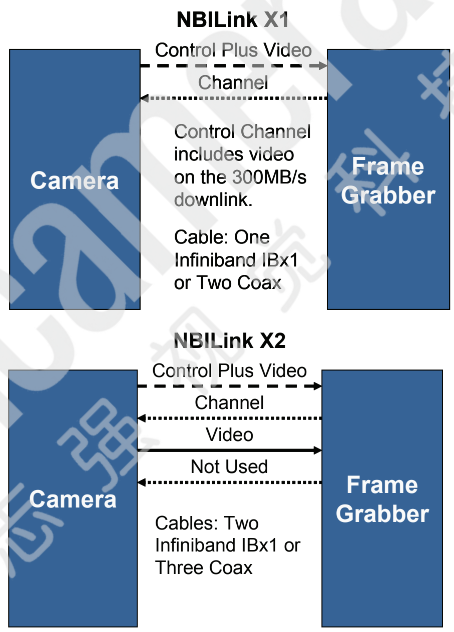


Figure 5 – NBILink x1 and x2 Configurations

Like NBILink, the MixedLink optimizes cable hardware by combining video with the downlink communications channel of the Control Channel. Thus, MixedLink provides a x7 solution on the same CX4 cable as GMIILink. Figure 6, shows the MixedLink configuration.

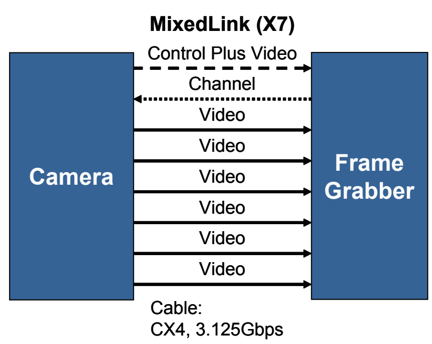


Figure 6 – MixedLink configuration

The current proposal is to run HSLink at a fixed 3.125 Gbps, thus ensure you purchase CX4 cables capable of handling this speed. The 3.125Gbps balances cost, throughput, transmission distance, power and simplifies the network discovery process.

Transmission Distance

Transmission distance and data reliability is a limitation and concern for Camera Link. HSLink improves upon both aspects. The CX4 copper cable solution, as specified by 10 GigE Ethernet, achieves 15 meter distances. Laboratory testing by DALSA has proven 20 meters is possible, and one IC vendor found 40 meters was possible. For those applications needing further transmission distance, HSLink is easily converted to fibre optic as it is 8b/10b coded and is suitable for direct conversion to fibre.

The PHY (Serdes)

HSLink uses Serdes IC chips (The PHY) that are widely available from multiple vendors. The Serdes chips serialize and deserialize the information sent between cameras and framegrabbers using proven 8b/10b encoding technology. To reduce IC chip count, the Serdes function can be incorporated into the latest mid tier/low end FPGAs without the need for external devices, enabling extremely small camera implementations. Also, IC and FPGA vendors continue to invest in 8b/10b technology, improving serial bit rates and power consumption for the foreseeable future. The HSLink protocol has been designed to take advantage of the upcoming improvements in Serdes technology. The Serdes IC chip is capable of handling both NBI and GMII protocols simultaneously for information exchange with the HSLink IP Core.

8b/10b encoding introduction

HSLink is built on proven 8b/10b data encoding technology. This encoding technology is the foundation of protocols known as PCIe, Gigabit Ethernet, 10-GigE, Infiniband, Fibre Channel, Serial Rapid I/O, CPRI and others. These protocols span the computer and telecommunication industries and enjoy large economies of scale and the associated large investments from IC vendors to improve the physical layer. HSLink is a protocol designed to meet the unique real time, extreme bandwidth range, and data reliability requirements of machine vision. As HSLink is designed for machine vision, no extra overheads are incurred and unique features of the protocol reduce the vision system design costs.

8b/10b is a method that converts 8 data bits into 10 bits that are transmitted serially. Of the 1024 patterns that are available, 256 are defined data patterns and an additional 12 patterns are defined as control words or Kcodes. These patterns have a +/- image known as the disparity. Essentially the disparity signifies if the pattern has 6 or 4 '1' bits in the 10 bit pattern. The motivation for adding the extra 2 bits for transmission is that it enables:

1) DC balance, which makes data recovery easier after long transmission lines.
2) Clock Recovery, ensures there are sufficient edges in the serial stream to enable the receiver to find the data clock and recover the serial bits that were sent.
3) Kcodes are unique patterns that enable the receiver to find the byte boundaries or other low level tasks. Most physical layer devices (phy) use the pattern known as K28.5 as the byte alignment pattern. Kcodes are also used at the protocol level to signal events like start of message, end of message.
4) The encoding/decoding method uses 2 small look up tables and is very cost effective.

Kcodes and Message Types

The afore-mentioned protocols all use the Kcodes, or control words, in different ways and each Kcode carries a different meaning in each protocol. Generally there is the concept of a start of packet, end of packet and idle characters. HSLink has chosen the idle Kcode that is most commonly used by the available phys today for byte alignment, ensuring machine vision companies have a wide number of vendors to choose from for implementation. Other available Kcodes are used to signify the start of a message type. Currently HSLink supports the following message types in priority order:

Priority Level	Message Type	NBI K-code
First priority level	Trigger	K28.2
Second priority level	GPIO	K28.4
Second priority level	Ack/Nack / Data Resend	K29.7
Third priority level	Video	K27.7
Fourth priority level	Command	K28.6
Fifth priority level	Idle	K28.5

Table 1 – Priority Levels and NBI K-Codes

HSLink IP Core

The HSLink IP Core is responsible for interfacing with the PHY and ensuring the correct information is sent between the framegrabber and camera. The essential functions of the HSLink IP Core are: priority management of the K-codes, data and trigger error handling and packet handling, as shown in Figure 7.

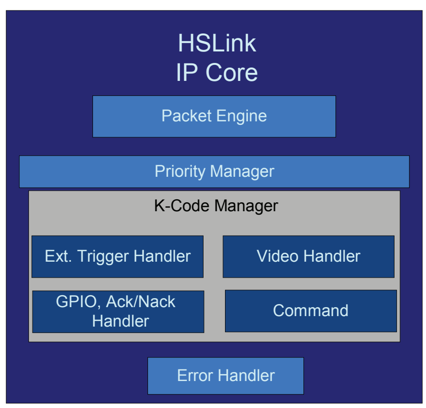


Figure 7 – System Diagram of HSLink IP Core

Priority Technology

The priority level of the message types is defined by the HSLink interface requirements and implemented by the HSLink packet engine arbitrator technology. The message priorities are shown graphically in Figure 8.

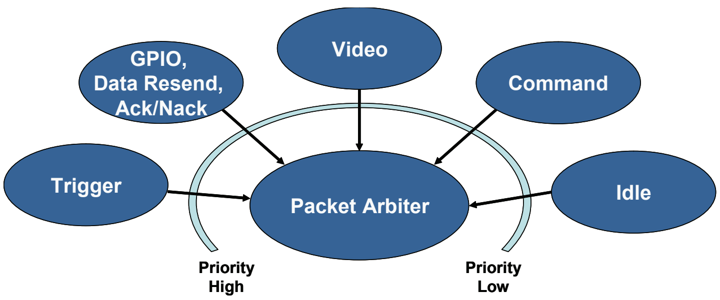


Figure 8 – Message priorities

HSLink uses a priority interrupt and continue packetization technology that maximizes the transmission bandwidth. The first-level priority technology achieves triggering jitter of 3.2ns and the second -level priority, GPIO messaging, achieves an uncertainty ranging from 3.2ns to 300ns depending on the trigger mode and other occurring activity. This 2nd level priority performance level is far superior to any available protocol today and will continue to outperform any generic computer based protocols since this level of performance is not needed by those industries. HSLink is designed to meet the high speed line scan trigger needs and high speed area trigger needs of tomorrow, today. The triggering and real time control capability make HSLink unique and will continue to be an advantage it brings into the future. Micro head cameras are possible with this technology as no extra trigger circuitry/connector is required in the cameras. HSLink is designed for a simple network, where it would be possible to install an I/O box and achieve real time control of peripheral devices from the frame grabber, or camera, such as LED strobes or air jets.

Data and Trigger Reliability

HSLink is targeted at critical customer product inspections where data errors can't be tolerated. To meet this need, the protocol has been designed to tolerate single bit error events at the rate of 10^{-12}, a typical specification for a PHY device. HSLink uses different methods to achieve reliability based on message type. The real time messages must be delivered without error the first time; there is no time to do a resend. The Trigger, GPIO, Ack/Nack are only a few bytes long and use 2 of 3 vote logic to overcome single bit errors. That is to say, all the bytes in the message are sent 3 times and the receiver considers the message to be received correctly when 2 of the 3 bytes are in agreement. The longer command and video messages use a CRC and data resend methodology to achieve data reliability.

A key feature for HSLink, which again enables low cost, small size, low power and simpler camera designs, when compared to software based protocols, is the hardware initiated video resend request. The real time error detection and request limits the amount of memory needed in the camera to successfully service a data resend request. Modern FPGAs easily accommodate the 4 rows of memory and the dual port feature of the memories simplifies the design of the resend memory controller.

CRC Calculation

The HSLink protocol is designed to support 1x to 20x or more data lanes real time. Traditional computer methods would require that the data be sent as one packet across all the lanes, ie a really wide and fast pipe. However, HSLink simplifies the approach and recognizes the limitations of FPGA implementation by calculating the CRC on a per lane basis, reducing the CRC calculation bandwidth to the 1x bandwidth of 312.5 Mhz which is easily achievable in the lowest speed grade of StratixII™, Virtex5™, or the highest speed grade of the Cyclone 3™. Newer generation FPGAs should be equally capable. Again HSLink simplifies implementation of bandwidth migration for the machine vision industry over the alternate approaches.

HSLink – Protocol

Two basic protocols are used within HSLink to address the wide range of camera and image processing needs in the machine vision industry, and to enable implementation with existing hardware today. The first protocol is called the NBI protocol and defines the protocol used in the Control Channel. It also handles video in low bandwidth implementations, such as NBILink, and in MixedLink. The Control Channel, which uses NBI protocol, is common amoungst all three Link types: NBILink, GMIILink and MixedLink. The second protocol is called the GMII protocol and is used on the GMIILink configuration of the CX4 connector. This variant is designed to support low cost image processing through the data forwarding capability to 5 slave frame grabbers. Additionally, the Control Channel of the GMIILink provides a bidirectional 300MB/s communication channel between slaves and the master framegrabber. See the Data Forwarding Configuration later in this primer. The Mixed protocol adds video information to the control channel of the GMIILink variant to maximize the video bandwidth on the single cable. Table 2 summarizes the link names and protocols used.

Link Name	Typical Configuration (Bandwidth)	Camera Control Channel Protocol	Video Shared with Control Channel	Video Lane Protocol
NBILink	X1 - X2	NBI	Yes	NBI
GMIILink	X3 - X6	NBI	No	GMII*
MixedLink	X7	NBI	Yes	GMII*/NBI

** GMII protocol enables low cost data forwarding*

Table 2 – Summary of Link names and associated protocols.

NBI (Nine Bit Interface) Protocol Overview

This protocol provides the command and low jitter trigger capability found in all HSLink variants. In lower bandwidth configurations this channel also carries video data. It derives its name from the interface to the physical layer device (PHY). The nine bits consist of 8 bit data and a K-code flag. The protocol has complete control over the K-codes and as such has designated specific Kcodes to start specific message types.

A key requirement for this channel to operate is that the camera must frequency lock to the frame grabber clock thereby enabling the low jitter trigger to be transferred from one end of the cable to the other end. This technique is used in the CPRI protocol found in cell phone base stations and enables the framegrabber FPGA to receive data from many cameras without the concern for the limited number of FPGA clock nets.

GMII (Gigabit Media Independent Interface) Protocol Overview

The GMII protocol defined in HSLink is based on the GMII protocol foundation that was developed for GigE applications. It defines the start kcode, stop kcodes and the idle sequence that is implemented by the PHY. The HSLink GMII protocol defines the number of preamble bytes, the header, the video data format, the CRC and the minimum number of idle bytes to support data forwarding to 5 slave framegrabbers.

This data forwarding is possible because GigE is designed to support small frequency variations at each end of the cable, and therefore the off the shelf phys include rate matching fifos. Additionally most off-the-shelf PHYs are able to loop the data that was received to the transmitter. These 2 features are used to advantage in the GMIILink as the cable bandwidth is asymmetric and the unused transmitters in the frame grabber are put to use by forwarding the data to a connector connected with a slave frame grabber.

NBI Packet Design

HSLink packet designs are tailored to the message types and are designed from the system perspective, keeping implementation costs low with today's technology.

- Packet segments are padded out to 32 bits. This simplifies the migration to higher speed serdes technology in the future as the 10 Gbps devices of today present a 32 bit wide interface.
- Specific Kcodes signify the start of a message. This makes it easy to steer the information to the intended function.
- No End of Packet Kcode is used. This enables a simple interrupt and continue priority engine and reduces packet overheads as messages are either a known length or include the number of bytes in the header.
- Packet Start Phase concept is used to simplify transmitter/receiver design. All messages except trigger, begin at the Packet Start Phase. The idle pattern is used to transmit the Packet Start Phase and is a key protocol feature that enables simple receiver design in terms of priority decoding and handling random bit errors in the link.
- Real time messages use triple redundant sending and a 2 of 3 majority vote in the receiver to tolerate single bit errors.
- Longer messages such as command or video use CRC and data resend techniques to handle bit errors.
- GMII video lanes include sequential packet ID used to detect dropped packets caused by single bit errors.
- Self contained video lanes - includes header and CRC per lane, enabling real time CRC calculation for 1 to 20 lanes.
- Messages of higher priority interrupt lower priority messages, but messages of the same priority wait for the completion of an "in transit" message.

Trigger Packet

Real time triggering is key to a successful machine vision link. HSLink achieves 3.2ns of jitter from one end of the cable to the other with today's technology. This level of performance is sufficient for the next 5 to 10 years and it is possible that FPGA fabrics will be able to run at 625 MHz in the future, thereby improving (reducing) the jitter without any change to the protocol.

HSLink triggering is built upon the concepts used in Camera Link but extends Camera Link and offers 8 standard triggering modes. This triggering flexibility ensures that camera needs are met now and into the future and standardized trigger definition enables ease of end customer use. The trigger packet is of the form.

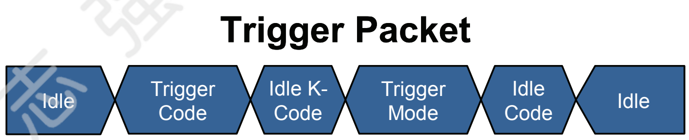


Figure 9 – Trigger Packet

GPIO Packet

The GPIO is a 2nd level priority packet and is used to send a signal level from one end of the cable to the other. Considering the GPIO packet uses the Control Channel running at 300MB/s, with HSLink GPIOs become suitable for real time control applications or for selecting camera operating modes that change row by row for line scan or frame by frame for area array. The status of these lines is returned with the video to help coordinate with the FG in applications such as on the fly windowing.

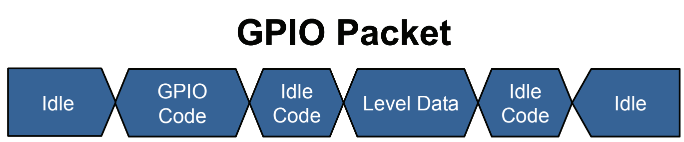


Figure 10 – GPIO Packet

Ack/Nack/Video Resend Packets

These 2nd level packets are used to acknowledge Control Channel communications and perform the flow control operation for the Control Channel. Included in this group of messages is the video resend request packet. Flow control for the Control Channel is needed because the HSLink communication bandwidth can be as high as 300 MB/s. This packet type has the form shown below.

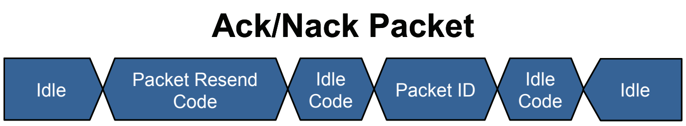


Figure 11 – Ack/Nack Packet

NBI Video Packet

Like Camera Link, the video data is “pushed” into the frame grabber. That is to say the frame grabber is responsible for keeping up to the camera, which minimizes the amount of memory needed in the camera head, reducing the system costs and head size.

The data presentation on the link is well defined to reduce the complexity of data reorganization and simplify frame grabber design and power on discovery process.

This is a third level of priority in the NBI protocol and shares the lane with command, GPIO and trigger information. The NBI video packet has form shown below.

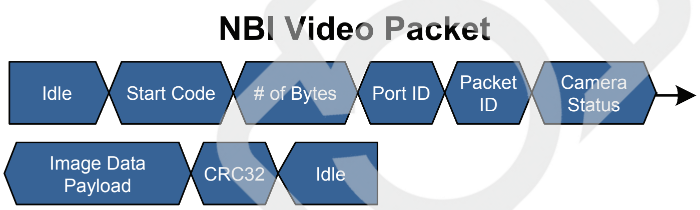


Figure 12 – NBI Video Packet

GMII Video Packet

Similar to the NBI Video Packet, the GMII video data is "pushed" into the frame grabber.

The data presentation on the link is well defined in order to reduce the complexity of data reorganization and simplify frame grabber design and power on discovery process.

The GMII video packet is used to send video data from the camera to the framegrabber over dedicated video data lanes. The GMII start and stop Kcodes are inserted by the PHY. The 16 preamble and minimum 16 idle bytes are defined by HSLink to support upto 5 slaves. The machine vision specific header is added after the preamble and uses a redundant data technique to ensure that the header is received correctly. CRC is used to detect errors in the data. The HSLink IP Core requests a data resend should an error in either the header or data be found.

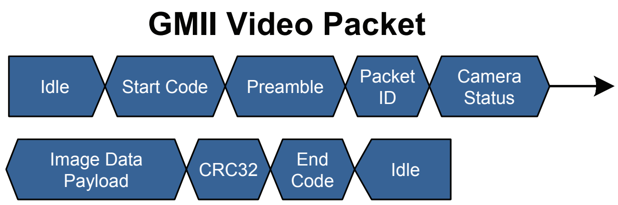
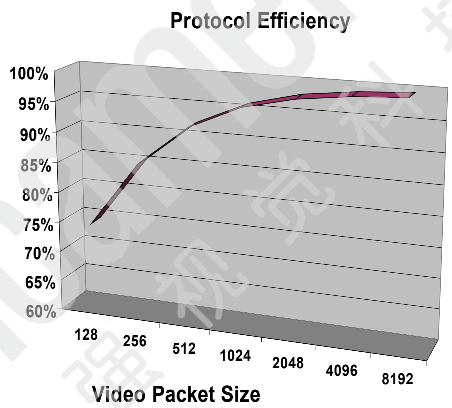


Figure 13 – GMII Video Packet

The following graph shows the protocol efficiency for the GMII video packet. The NBI video packet is slightly more efficient.



Graph 1 - GMII Protocol Efficiency

Command Packet

The command packet has 4th level priority. It is used to send information to the camera/frame grabber like the serial link in Camera Link. As the protocol is designed to support intermediate devices between the camera and frame grabber, there is the need to include a target address. The network architecture supported by HSLink is very simple in order to keep the addressing overheads small and the software support for the network easy to implement. Also, HSLink supports the camera initiating a communication with the framegrabber. The Packet is represented below.

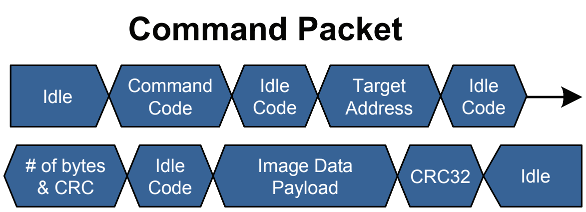


Figure 14 – Command Packet

Idle Set

Idle sets are inserted anytime there is no useful information to transfer. The GMII video data lanes have Idle sets that are inserted by the PHY and require a minimum clock count between packets. The NBI idle sequence is a set of 4 bytes which consists of 3 K28.5 characters and a configuration byte. All NBI packet starts are phased to a 4 byte boundary except the trigger which can start at any phase for reduced jitter. This technique is used to simplify the receiver design. The configuration byte includes HSLink revision and if the device is a master/hot standby, camera or intermediate device. Setting the configuration byte to zero resets the far-end link receiver. The following drawing shows the NBI Idle packet format.

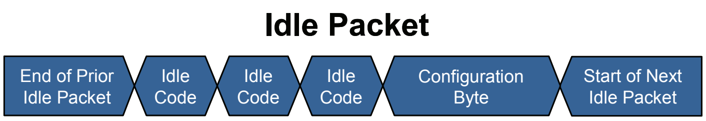


Figure 15– Idle Packet

System Configurations
Multiple Cameras to One Framegrabber

HSLink protocol is designed to support up to 64 cameras from a single framegrabber. The following figure shows a number of NBILink based camera connected directly to a framegrabber.

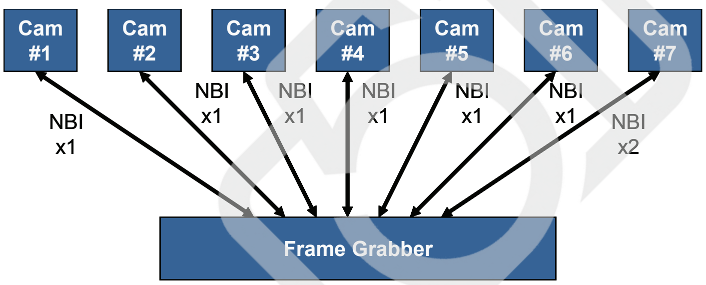


Figure 16 – Multiple Cameras to One Framegrabber

Data Forwarding

HSLink recognizes that data transmission is only part of the system requirements and has been architected to support multiple parallel processing nodes. The NBI protocol and data presentation makes possible the splitting of an image into vertical stripes splitting out the data lanes to multiple 1x framegrabbers. The MixedLink or GMIILink mode is used when the entire image is to be forwarded to each processing node. This forwarding of data is accomplished with the addition of a connector and short cable, ie low cost. The following figure illustrates data-forwarding where 6 framegrabbers are used to process the imaging data from one (very fast) camera.

HSLink Data Forwarding Topology

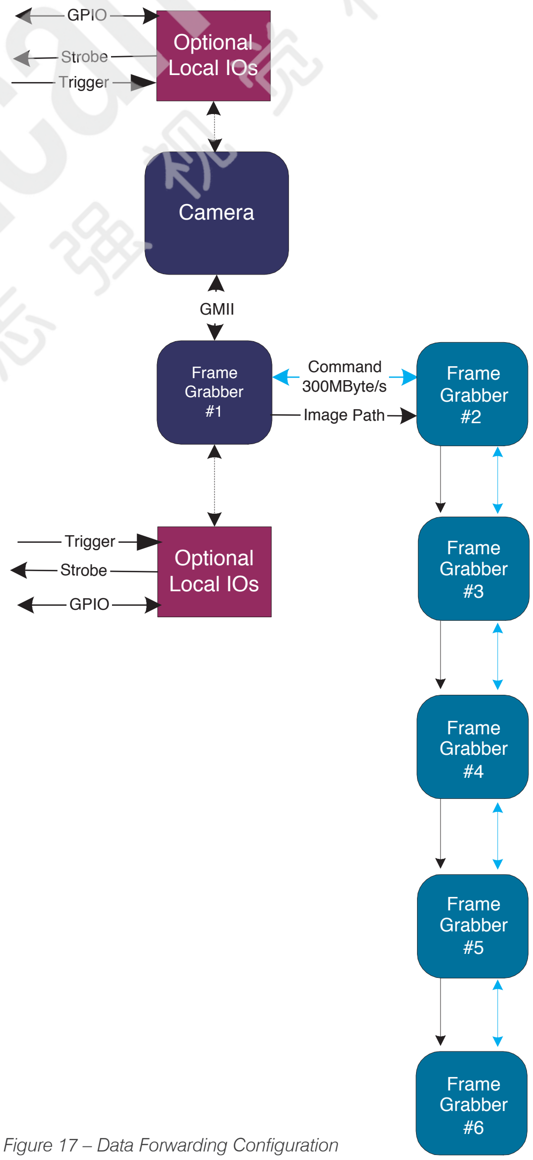


Figure 17 – Data Forwarding Configuration

Image Path
GMII = 1800MBytes/s
Mixed Mode = 2100MBytes/s

Intermediary Devices

The protocol is designed to support intermediate devices installed between a camera and frame grabber. The functions offered by this intermediate device might include a GPIO box, data concentrator or data replicator for high reliability systems. The protocol is designed to support up to 64 cameras from a single frame grabber. The figure below shows a 2 to 1 concentrator application. This flexibility meets the needs of most machine vision systems.

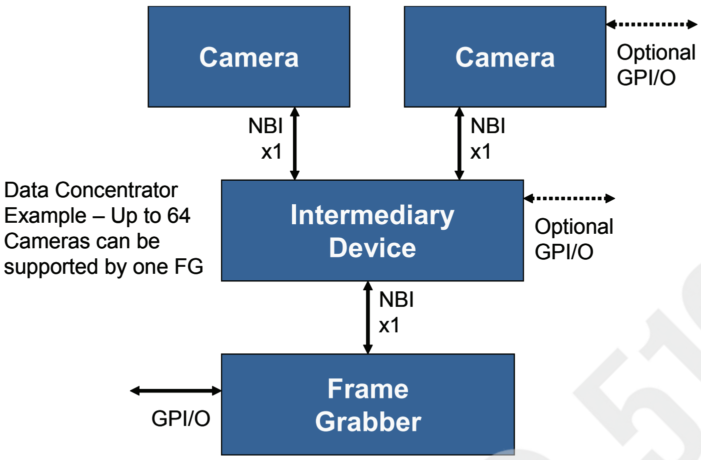


Figure 18 – Intermediary Device Example

HSLink Comparison to Other Interfaces

HSLink is designed to be an upgrade for Camera Link, enabling smaller, lower cost cameras and frame grabbers, connected over simple network topologies found in the machine vision market. HSLink enables very high camera bandwidths on a single cable and offers a low cost data forwarding mode to reduce image processing costs. Data reliability has been a key design requirement for HSLink and hardware resend simplifies camera design. The key concepts of Camera Link have been migrated to HSLink with improved capabilities with a goal of achieving a plug and play experience.

The following table compares HSLink against Camera Link, GigE,10GigE and CoaXpress which are implementable today. Future standards such as USB 3 or higher speed Firewire, or consumer/computer video standards lack some of the triggering and data resend capabilities needed for reliable inspection systems. Some information regarding the capabilities of CoaXpress was not available at the time of print. It is known that the phy used in CoaXpress is currently single sourced and the technology can not be integrated into an FPGA.

HSLink is ideal for the camera designer at any bandwidth because it delivers to the customer a small imaging head, reliable and low cost data transmission technology, and ease of use with standardized triggering and GenIcam compliance. Camera manufacturers can differentiate their product by adding external GPIO connectors, or add other image processing features within the camera. Power dissipation and cost are minimized by the asymmetric bandwidth and the ability to add bandwidth in 300 MB/s increments.

Feature	HSLink	Camera Link	10GigE	GigE	CoaXpress
Bandwidth	6000MB/s	850MB/s	1200MB/s	100MB/s	1,200MB/s
Scaleability	NBI 1x-300MB/s, and multiples GMII/Mixed- upto 2100 MB/s in steps of 300MB	Lite 150MB/s, Base 255MB/s, Medium 510MB/s, Full 680MB/s, Full 850MB/s+	4x- 1200 Multiples	Multiple of 100MB/s with additional connector/cable.	1x -300 MB/s and multiples of 300 MB/s
Trigger	3.2ns jitter	0 ns jitter	1us IEEE1588 (special hardware required)	1us IEEE1588	12ns jitter
Distance	15m on CX4 80m on RG59	10m	15m-CX4 100m-Cat7	100m- Cat 5e	105 m
Fibre Optic	Yes	No	CX4- Yes	No	No
Number of Cameras from 1 FG	8- 1x cameras	2 (4)	2	4	5
High Speed Camera Control (CC) Lines	8	4	0	0	0
Network Support	Yes- 64 Cameras	No	Yes	Yes	No
Data Forwarding/ Replication	Mixed and GMII modes and/or via Data Replicator	Via Data Replicator	Via Hub and broadcast message	Via Hub and broadcast message	Data Forwarding via Data Replicator
Com Channel	300 MB/s	1MB/s	1200MB/s	100MB/s	2.1MB/s
Integrate phy into FPGA	Yes	Yes	Yes, CX4	No	No

Table 3 – HSLink Comparision to Other Interfaces

Appendix A – Contact Names

If you have any questions or feedback on HSLink, or any corrections on questions on this primer, please direct these to:

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Appendix B – Terminology

Control Channel – Two wire pairs forming a bidirectional communcation channel.

Lane – A single wire pair forming a unidirectional data path used for video data.

Link – A collection of one control channel and 0 through 20 video lands. There is only one control channel per link and it can support video data in some variants.

KCodes – The 8b/10b coding standard supports 256 data codes and 12 control characters or Kcodes. The control characters are used to signify packet start, channel idle, or other message events while other characters are used by the PHY chips to maintain link operation.

8b/10b Data Encoding – See 8b/10b encoding introduction section.

CRC – Cyclic Redundancy Check - See CRC calculation section.

NBI – Nine Bit Interface – See NBI (Nine Bit Interface) Protocol Overview section.

GMII – Gigabit Media Independent Interface – See GMII (Gigabit Media Independent Interface) Protocol Overview section.

SERDES - A serializer/deserializer is an integrated chip (IC) the converts parallel data into serial data and vice-versa. Multiple SERDES chips are commonly housed in one IC.

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