The Evolution of CMOS Imaging Technology

Innovations and improvements in CMOS imaging technology design and fabrication have allowed designers to overcome many traditional practical implementation issues. Although integrated circuit design is always a process of optimizing tradeoffs between limiters, CMOS imaging technology designers can now deliver products with performance that is truly compelling for machine vision applications. With these innovations and considerable time and investment, CMOS imaging technology has seen significant advancements and has increased in usage over competing CCD technology by original equipment manufacturers in the machine vision industry.

Choosing the most suitable camera for a specific machine vision application requires a delicate balancing of different attributes of the image sensor and camera with the needs of the machine vision system. The progress that has been made in CMOS technology over the past decade has made it the preferred technology for high speed inspection.

Three main attributes define the primary set of trade-offs for an area imaging device. The first set of attributes can be observed in imaging performance: image quality, maximum number of frames per second, and resolution. The second set of trade-off attributes is in the functionality of the camera or sensor, where competing features call for difficult decisions. Examples of these secondary trade-off attributes include features such as windowing and power consumption. Finally, there are feasibility trade-offs to be made which deal with cost, yield, reliability and other features related to the manufacturing of the imaging device.

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Figure 1: CMOS Image Sensor Primary Trade-off

Although in the past the image quality thresholds required the use of ILT CCD sensors (inter-line transfer CCD) in many applications, improvements in the design of CMOS sensors have led to better image quality and opened up new possibilities for much faster inspection systems with the desired image quality. Historically, CCD ILT technology was the dominant sensor technology for shuttered imaging. The first generation of CMOS technology entered the market offering only rolling shutter functionality, which precluded its use in most shuttered applications despite the opportunity for higher speed, lower power, and lower cost. Later on, the CMOS global shutter feature was introduced, solving the rolling shutter shortfall and allowing CMOS to be relevant to more users. Recent advances in the technology have vastly reduced the noise and improved signal to noise ratio (SNR) levels, in CMOS. CMOS technology surpasses what is possible in the CCD ILT, which was the last of the major performance hurdles. In high speed machine vision applications, CMOS meets or exceeds CCD ILT technology in functionality, performance, and cost.

The latest generations of CMOS imaging technology have diminished the trade-off between resolution and speed by using very high data throughput, made possible by very fast, high bandwidth analog to digital converters. The speed of these devices has challenged the boundaries of available data transmission standards such as CameraLink and has been the primary driving force behind the new high bandwidth CameraLink HS standard.

Advances in pixel structures, such as global shutter pixels, have already narrowed the gap between speed and image quality that has been an issue in high speed applications in the past. This technology is currently a de facto standard for any high end CMOS image sensor.
implementation of the device. One of the main focuses of CMOS technology development in the past has been to overcome image artifacts. The user must pay close attention to the performance of a CMOS image sensor with regard to image artifacts arising in extreme situations or certain operation and lighting situations. This consideration heavily impacts a designer’s decision when faced with design trade-offs. A sensor that has excellent combinations of specifications may prove to be unusable if it exhibits image artifacts.

Some of the major trade-off parameters are explained below:

A) Fill Factor
There is an inverse relationship between the number of transistors in a given pixel and its fill factor. Fill factor, the percentage of light sensitive area in a pixel, directly impacts the sensitivity of a sensor and S/N of the captured image. On the other hand, having more transistors in a pixel allows for additional features, such as global shutter and correlated double sampling (CDS) that enhance image quality.

B) Light Acceptance Angle
In order to minimize the impact of increased number of transistors per pixel, most CMOS image sensors use micro lenses. A micro-lens compensates for some of the lost real estate in a pixel due to increased number of transistors. However, micro-lenses reduce the “light acceptance angle” in a pixel. The use of micro-lenses somewhat improves the trade-off between the number of transistors in a pixel and image quality.

C) Pixel Charge Capacity (Qsat) and Maximum Exposure Level
Another major drawback of having more transistors in a pixel is reduced pixel charge capacity. In addition, a reduction in pixel size (increased resolution for the same size sensor), means less space for charge storage, which in turn results in lower pixel charge capacity. Reduced pixel capacity directly impacts the suitability of sensors for some applications. For example, many applications require the camera to differentiate between shades of grey in a bright image. In these applications, shot noise is the decisive factor and not the absolute noise floor. Since the signal to noise ratio in the shot noise limit scales with the square root of the captured photon signal, shot noise limited applications require high pixel storage capacity. Higher pixel storage capacities also help to minimize the size and impact of several types of imager non-idealities such as blooming and parasitic image artifacts
An alternative approach to the "voltage domain" global shutter structure is a "Charge Domain" structure, where the transfer of the image into shielded area takes place in the "Charge Domain." This vastly reduces the complexity of the pixel but requires optimized implementation of the components within a pixel. To achieve a better trade-off scheme between global shutter and other performance parameters, CMOS fabrication process challenges must be met and overcome. Essentially, with this method, a reduced number of high quality elements in the pixel achieves the same result as a more complex pixel circuitry.

**Conclusion**

There are several competing factors at play in the CMOS imaging device design process. Some of the trade-offs are fundamental and related to the physics of operation of the device, while others are due to practical non idealities in the implementation of the design. A good CMOS imaging device design should consider all of these factors in order to come up with an optimal design. Future generations of CMOS technology will certainly continue to enhance the performance of imaging devices. Now users can benefit from both high resolution and high speed imaging devices that provide image quality that exceeds application requirements. Future generations of CMOS technology will defy today’s limits with unprecedented combinations of imaging device attributes.

**Meet the authors**

Behnam Rashidian is Senior Product Manager and Eric Fox is Technical Director CMOS ICs at Teledyne DALSA in Waterloo, Ontario, Canada.

emails: behnam.rashidian@teledynedalsa.com, eric.fox@teledynedalsa.com

www.teledynedalsa.com